TY Electronics
Semester V

Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

AY 2025-26

Course Information	
Programme	B. Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem V
Course Code	7EN301
Course Name	Digital Signal Processing
Desired Requisites:	Signals and Systems

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
		30	20	50	100
		Credits: 3			

Course Objectives	
1	To illustrate the fundamental concepts of Digital Signal Processing.
2	To explain the different techniques for design of filters and multirate DSP systems.
3	To enable the students for the design and development of DSP systems.

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Solve Discrete Fourier Transform in efficient manner	Evaluate
CO2	Analyze the structures for Discrete Time systems	Analyze
CO3	Design the FIR, IIR Digital Filters with given specifications	Create
CO4	Describe the fundamentals of Multi rate DSP and Wavelet Transform	Understand

Module	**Module Contents**	**Hours**
I	**Discrete Fourier Transform and its Computation:** The Discrete Fourier Transform and its Properties, Efficient Computation of the Discrete Fourier Transform, Decimation-in-Time FFT Algorithms, Decimation-in-Frequency FFT Algorithms, Implementation of FFT Algorithms for IIR Systems, Lattice Structures	**7**
II	**Structures for Discrete-Time Systems:** Introduction, Block Diagram Representation of Difference Equations, Signal Flow Graph Representation of Difference Equations, Basic Structures of FIR Systems, Basic Network structures	**5**
III	**Filter Design Techniques-FIR Filters:** Introduction, Design of FIR Filter by Windowing, Properties of commonly used windows, Linear Phase property of FIR Filter, Kaiser Window Filter design, Discrete Time Differentiator	**8**
IV	**Filter Design Techniques-IIR Filters:** Introduction, Design of Discrete-time IIR Filters from Continuous-time Filters, Filter Design by Impulse Invariance, Filter Design by Bilinear Transformation, Frequency Transformations of Low pass IIR Filters	**7**
V	**Multi rate Digital Signal Processing:** Introduction, Decimation and interpolation, Sampling rate conversion, Multistage Implementation of Sampling rate conversion, Sampling rate conversion for Band pass signals, Sampling rate conversion by arbitrary factor, Applications of Multi rate DSP	**7**

VI	**Introduction to Wavelet Transform:** STFT, Wavelets representation, Haar Wavelet, Daubachis Wavelet, Filter Bank representation	**5**
Textbooks		
1	"Digital Signal Processing", Sanjit K. Mitra Tata McGraw-Hill Publication 4th edition	
References		
1	"Advanced Digital Signal Processing", J. G. Proakis, Prentice Hall India, 2007	
Useful Links		
1	NPTEL	

	CO-PO Mapping													
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													2
CO2		3												2
CO3				2										2
CO4	2													2

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2025-26

Course Information	
Programme	B. Tech. (Electronics Engineering)
Class, Semester	2025-26 Year B. Tech., Sem V
Course Code	7EN302
Course Name	Embedded System Design
Desired Requisites:	Microcontroller Peripherals and Interfacing theory and lab

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial		30	20	50	100
		Credits: 3			

Course Objectives	
1	To illustrate the features of ARM architecture.
2	To provide the knowledge of different hardware peripherals and programming of different peripherals of ARM7 based controller. Ex. LPC2148 / LPC1768
3	To empower the students for the design and development of embedded system.
4	To encourage students to provide solution for real world problems using embedded systems .

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Illustrate architecture and operation of internal peripherals of ARM microcontroller	Apply
CO2	Write assembly and C program to configure and use internal peripherals ARM microcontroller	Apply
CO3	Analyse program and find operating parameters of peripheral in ARM microcontroller.	Analyse
CO4	Design and develop small embedded system using embedded C programming and ARM microcontroller.	Create

Module	**Module Contents**	**Hours**
I	**Architecture** ARM7 / ARM Cortex M3 Architecture, Memory organization, Programmers model, Pipelining, Memory, Register Structure, Current Program Status Register, Exception Modes, System buses and peripherals, Memory Accelerator module, Compare features / architecture of ARM with 8051	6
II	**Embedded C Programming** Introduction to ARM7 / ARM Cortex M3 programming example, Software documentation method, Development Tools, ARM C Programming, Startup code, microcontroller pin layout, PLL configuration, Pin Connect block, I/O programming, boot-loader, In Application Programming. External Peripheral Interfaces like led, switch, LCD, Motor, Seven Segment Display etc.	8
III	**Interrupt Structure of ARM Microcontroller** Interrupt system in ARM7 / ARM Cortex M3, Interrupt Controller, FIQ, IRQ, Non-vectored interrupt, Software interrupt, Interrupt latency, Nested interrupts, External interrupts, Interrupt configuration and Programming examples	6

IV	**Peripherals of ARM Microcontroller** Block diagram of Timers, role of prescaler, Capture and Match facility of timer and configuration of it using registers, Pulse Width Modulator, RTC operation and Programming, Watch dog timer, Analog to digital converter, Digital to analog converter and their programming	8
V	**Communication Protocols** On chip serial ports, Serial port programming, setting baud rate, Using UART buffer, printf for serial data transfer, interrupt based serial port handling, I2C protocol, Using I2C for interfacing external EEPROM, SPI protocol and programming.	7
VI	RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multi processing and Multi-tasking, Task Scheduling.	4

Textbooks	
1	Andrew Sloss, ARM System Developer's Guide, Elsevier India, 2005
2	Joseph Yiu, "The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors", Newnes; 3rd edition
3	"Textbook of EMBEDDED SYSTEM", NA. VIKRAMAN
4	"Introduction to Microprocessor Based Systems Using the ARM Processor" by Kris Schindler
5	Embedded Microcomputer Systems – Real Time Interfacing – Jonathan W. Valvano; Cengage Learning; Third or later edition.

References	
1	ARM inc, ARM Reference Manual, ARM, inc., NA, 2011
2	Technical references, data sheets and user manuals of respective controller
3	Yifeng Zhu, "Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C", E-Man Press LL
4	Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
5	Embedded Microcomputer Systems – Real Time Interfacing – Jonathan W. Valvano; Cengage Learning; Third or later edition.

Useful Links	
1	https://nptel.ac.in/
2	https://in.coursera.org/
3	https://www.nxp.com/
4	https://www.arm.com/
5	http://www.embeddedworld.com/

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2	3													
CO3		3			3									
CO4			3											

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2025-26

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem. VI
Course Code	7EN303
Course Name	CMOS Digital VLSI Design
Desired Requisites:	Digital Electronics, Electronic Circuits Analysis and Design, Microelectronics

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	2 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	1 Hrs/week	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives	
1	***Explain*** the long and short channel MOS transistor models with emphasis on unified model.
2	***Explain*** the steps involved in manufacturing process of MOS devices.
3	***Explain*** the considerations in optimizing the physical dimensions of MOS transistors in obtaining the trade-off between area, speed and power requirements of CMOS based systems.
4	***Develop*** the logical and design skills of CMOS combinational and sequential logic circuits.

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	**Explain** the basic steps with theoretical principles involved in the process of manufacturing of CMOS devices.	Understand
CO2	**Model** sub-micron, deep submicron MOS transistors and Interconnects.	Apply
CO3	**Analyze** the fundamental principles involved with MOS devices to **design** CMOS inverter to meet the area, speed and power requirements.	Analyze
CO4	**Design** static and dynamic CMOS Combinational Logic circuits and Sequential Logic Circuits by considering the performance parameters like area, speed and power.	Create

Module	**Module Contents**	**Hours**
I	**MOS Transistor Theory** MOS Transistor under Static Conditions, Dynamic Behaviour, Secondary Effects, SPICE Models for MOS Transistor, Technology Scaling.	3
II	**Manufacturing Process for CMOS ICs** Photolithography, Design Rules, Packaging Integrated Circuits, Thermal Considerations in Packaging.	2
III	**CMOS Inverter** Static and Dynamic Behaviour of CMOS Inverter, Power and Energy-Delay, Impact of Technology Scaling on Inverter Metrics.	6
IV	**CMOS Combinational Logic Circuits** Static CMOS Logic Design, Dynamic CMOS Logic Design, Comparison between the two Design Styles.	6
V	**CMOS Sequential Logic Circuits** Static Latches and Registers, Dynamic Latches and Registers, Pulse Registers, Non-Bistable Sequential Circuits: Schmitt Trigger Circuit, Ring Oscillator, Voltage Controlled Oscillator.	5

VI	**Interconnect and Semiconductor Memories** Electrical Models of Wires, Lumped RC Model, Distributed rc line, Transmission Line; Memory Classification, Memory Architectures and Building Blocks, Memory Core: ROM, RAM.	4

Text Books	
1	Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits-A Design Perspective", 2nd Edition, Prentice-Hall India Learning Pvt. Limited/ Pearson Education, 2014.
2	Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", 3rd Edition, McGraw-Hill Education (India) Pvt. Ltd., 2015.
3	
4	
References	
1	Neil Weste, Kamran Eshraghian, "Principles of CMOS VLSI Design: Analysis and Design", Addison Wesley/Pearson Education, 2008
2	William Dally and John Poulton, "Digital System Engineering", Cambridge University Press, Reprint 2007.
3	
4	
Useful Links	
1	https://nptel.ac.in/courses/108/107/108107129/
2	https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-374-analysis-and-design-of-digital-integrated-circuits-fall-2003/index.htm
3	
4	

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	2													1
CO2			2											1
CO3		3	2											2
CO4		2	3											2

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2025-26

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem V
Course Code	7EN351
Course Name	Digital Signal Processing Lab
Desired Requisites:	Signals and Systems

Teaching Scheme		**Examination Scheme (Marks)**			
Practical	2 Hrs/ Week	**LA1**	**LA2**	**Lab ESE**	**Total**
		30	30	40	100
		Credits: 1			

Course Objectives

1	The objective of the course is to work out for the convolution, correlation, DFT, IDFT, Block convolution, Signal smoothing, filtering of long duration signals, and Spectral analysis of signals using MATLAB simulation

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Identify the basic operations of Signal processing	Analyze
CO2	Resolve the spectral parameter of window functions	Analyze
CO3	Design IIR, and FIR filters for band pass, band stop, low pass and high pass filters	Create
CO4	Study of up sampler and down sampler in time and frequency domain	Analyze

List of Experiments / Lab Activities/Topics

List of Lab Activities:

1. Generation of different signals using MATLAB
2. Calculate FFT AND plot Magnitude and Phase response for the same
3. Find circular convolution of given sequences
4. Implementation of Moving average filter
5. Implementation of Median filter
6. Overlap and save method illustration
7. Design of simple filter
8. Design of FIR filter
9. Observe the effect of length of filter on the magnitude response of a filter
10. Design of FIR filter using different window functions
11. Design of FIR filter using Kaiser window
12. Illustration of up sampling of signal
13. Illustration of down sampling of signal

Textbooks

1	"Digital Signal Processing", Sanjit K. Mitra Tata McGraw-Hill Publication

References

1	Advanced Digital Signal Processing", J. G. Proakis, Prentice Hall India.

Useful Links	
1	NPTEL

CO-PO Mapping														
	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													2
CO2		3												2
CO3				2										2
CO4	2													2
The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High Each CO of the course must map to at least one PO, and preferably to only one PO.														

Assessment				
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%				
Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40
Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.				

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AY 2025-26

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	25-26 Year B. Tech., Sem V
Course Code	7EN352
Course Name	Embedded System Design LAB
Desired Requisites:	Microcontroller Peripherals and Interfacing theory and lab

Teaching Scheme		**Examination Scheme (Marks)**			
Practical	2 Hrs/ Week	**LA1**	**LA2**	**Lab ESE**	**Total**
Interaction		30	30	40	100
		Credits: 2			

Course Objectives

1	Write, simulate and debug assembly and C programs for LPC2148 / LPC1768 microcontroller
2	Write, simulate, download and test C programs for microcontroller using development board
3	Develop C program for implementing given or required system operation.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Apply programming skills to integrate hardware peripherals of ARM microcontroller.	Apply
CO2	Test and debug programs for ARM microcontroller.	Analyse
CO3	Develop and demonstrate small embedded systems using ARM C programming and hardware peripherals for ARM microcontroller.	Create
CO4		

List of Experiments / Lab Activities/Topics

List of Topics (Applicable for Interaction mode):

List of Lab Activities:

List of Experiments:

1. Experiment 1: Introduction of the development tools and kit
2. Experiment 2: Simple assembly language, embedded C program and study of startup.s file
3. Experiment 3: GPIO Programming
4. Experiment 4: PLL Programming
5. Experiment 5: Interrupt programming (IRQ and NV-IRQ)
6. Experiment 6: FIQ programming and comparison of FIQ with VIRQ and NVIRQ
7. Experiment 7: Programming Timer as Timer and Timer as Counter
8. Experiment 8: Programming Timer to perform capture operation and match facility of timer
9. Experiment 9: Programming PWM and application of it
10. Experiment 10: Programming ADC and DAC
11. Experiment 11: Programming UART
12. Experiment 12: Programming RTC and WDT
13. Experiment 13: Introduction with Basic RTOS programming.
14. Mini-Project

Textbooks

1	NXP, LPC 2148 / 1768 data sheet, NXP inc.,

2	NXP, LPC 2148 / 1768 user manual, NXP inc.,
3	Development board / Kit reference manual
4	
References	
1	Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication
2	Joseph Yiu, “The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors”, Newnes; 3rd edition
3	Technical references and user manuals of respective controller
4	Embedded Microcomputer Systems – Real Time Interfacing – Jonathan W. Valvano; Cengage Learning; Third or later edition.
Useful Links	
1	http://www.arm.org/
2	http://www.embeddedworld.com/
3	http://nptel.ac.in/
4	http://www.iitd.ac.in/

CO-PO Mapping														
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3				2									2
CO2		3												2
CO3			3									2		2
The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High Each CO of the course must map to at least one PO, and preferably to only one PO.														

Assessment				
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%				
Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40
Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.				

Walchand College of Engineering, Sangli

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AY 2025-26

Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem. VI
Course Code	7EN353
Course Name	CMOS Digital VLSI Design Laboratory
Desired Requisites:	Digital Electronics, Electronic Circuits Analysis and Design, Microelectronics

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	2 Hrs/Week				
Interaction	-	**Credits: 1**			

Course Objectives

1	Demonstrate the flow of EDA tools (Cadence/ Microwind) for designing CMOS digital circuits. a) Cadence Tools (Schematic entry to simulation) b) Microwind for designing digital circuits (at physical level/ layout of CMOS circuits).
2	
3	
4	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Design** and **Simulate** schematics of CMOS circuits using Cadence/ Microwind tools.	Create
CO2	**Design** and **Simulate** physical layouts with optimum area for CMOS gates, pass-Transistors, Transmission gates, Combinational and Sequential Logic Circuits using Cadence/ Microwind tools.	Create
CO3		
CO4		

List of Experiments / Lab Activities

List of Experiments :

Using Cadence/ Microwind Design Tools:

1. MOS Transistor (NMOS and PMOS) characterization.
2. Implementation of CMOS inverter and its characterization for VTC and power for equal area and equal delay approach.
3. Implementation of 2-input NAND and NOR gate.
4. Implementation of AND gate and OR gate using pass transistors logic and transmission logic.
5. Implementation of Ring Oscillator Circuit and Schmitt Trigger Circuit and.
6. Implementation of 1-bit RAM/ ROM using MOS transistors.

Text Books

1	Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits- A Design Perspective", 2nd Edition, Prentice-Hall India Learning Pvt. Limited/ Pearson Education, 2014.

2	Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, 3rd Edition, McGraw-Hill Education (India) Pvt. Ltd., 2015.
References	
1	Cadence Manual
2	Microwind Manual
Useful Links	
1	https://www.cadence.com/en_US/home.html
2	https://www.microwind.net/
3	https://www.ni2designs.com/microwind.html
4	https://studylib.net/doc/15236608/microwind-user-manual-v1

CO-PO Mapping														
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1			3	2	3									3
CO2			3	2	3									3
CO3														
CO4														

Assessment				
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.				
Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40
Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.				

Assessment Plan based on Bloom’s Taxonomy Level				
Bloom’s Taxonomy Level	**LA1**	**LA2**	**Lab ESE**	**Total**
Remember				
Understand				
Apply				
Analyze				
Evaluate				
Create	**30**	**30**	**40**	**100**
Total	**30**	**30**	**40**	**100**

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AY 2025-26

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem V
Course Code	7EN311
Course Name	Program Elective: 1 Linear Algebra and Statistics
Desired Requisites:	Applied Mathematics I & II

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial		30	20	50	100
		Credits: 3			

Course Objectives

1	To provide the students understanding of Linear transformations, Matrix algebra, Vector space, Inner product of vector space.
2	To prepare students to solve systems of linear equations and counting problems.
3	To illustrate applications of Linear Algebra in Electrical networks, Control systems and computer graphics.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	understand Linear transformations for solving systems of linear equations and use Matrix algebra for solving linear equations	Understand
CO2	To understand Eigen values and eigen vectors and its application in solving electronic circuits.	Understand
CO3	manipulate sets and events, solve counting problems and determine the distributions of random variable.	Apply
CO4	Analyse basic statistical concepts and apply it on random data and use of standard R. V. models, in solving problems in Electronics engineering	Analyze

Module	**Module Contents**	**Hours**
I	**Systems of Linear Equations** Vectors and Linear combinations, linear transformations, solving systems of linear equations, Echelon and reduced echelon form, Matrices, Elimination using matrices, rules for matrix operations, the inverse of a matrix, characterization of invertible matrix, partitioned matrix, matrix factorization	7
II	**Vector Spaces** Vector spaces and subspaces, null space, Column and row spaces, Dual space, transformations, linearly independent sets, bases and dimension, coordinate systems, applications to Electrical circuits and data smoothing	7
III	**Eigen values and eigen vectors** Eigenvalues and eigen vectors, characteristic equations, linear transformations, diagonilzations, Applications to systems of linear differential equations, complex eigen values, Inner-product spaces, orthogonality, least squares approximations	7

IV	**Probability and Random Variables** Sample space, outcomes, and events, axioms of probability; unions, intersections, and complements; Conditional probability, Total Probability law, Bay theorem, Random variable, Discrete and Continuous R.V. Density and distribution of function of single random variable, Properties of PDF and CDF. Some Standard R. V. like Bernoulli's, Binomial, Poisson, Geometric, Uniform, Exponential and Normal distribution Its application in electronics engineering. – representation, classification, Linear, Time invariant, causal, BIBO stable, Static, dynamic, memoryless, Convolution	10
V	**Multiple Random Variables and Moments** Two-dimensional random variable, Joint PDF, and CDF. Expectations and Higher order moments, Central moments, Variance, Moment generating functions Joint Moments., Covariance.	6
VI	**Correlation and Regression** Correlation. Properties of correlation coefficient, Conditional Expectation, Lines of regression, coefficient of correlation of bivariate data, regression curves	5

Textbooks	
1	Introduction to Linear Algebra: 4th edition, Gilbert Strang, Wellesley-Cambridge Press, 2009
2	Higher Engineering Mathematics, B.S.Grewal, Khanna Pub
3	Probability and Statistics, P. Kandaswamy and K.Gunawati. S. Chand Publications
4	Probability and Queuing Theory by K. Prabha SciTech publication

References	
1	Linear Algebra Theory and Applications: Ward Cheney and David Kincaid, Jones and Bartlett publishers, Indian Edition 2010 2. 3. 4. 5.
2	Probability and Statistics with reliability, queuing and computer applications, K.S.Trivedi, Printice Hall India.
3	Probability Theory and testing of hypothesis CBT Package from Sonaversity Salem 636005
4	Probability models, Shieldon Ross, TMS
5	"Probability and Stochastic processes: a friendly introduction for electrical and computer engineers," Yates and Goodman, John Wiley, 2nd edition

Useful Links	
1	

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1		3												
CO2	3	3												2
CO3	3				2									1
CO4		2	2										2	1

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

AY 2025-26

Course Information	
Programme	B. Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem.-V
Course Code	7EN312
Course Name	Professional Elective-1: Control Systems
Desired Requisites:	Calc, diff equations, linear algebra, and complex numbers

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial		30	20	50	100
		Credits: 3			

Course Objectives	
1	To provide with the necessary information regarding sensing of various parameters, Data Acquisition System required in the industries
2	To provide fundamentals of Control systems such as open loop and closed loop systems, Block diagram, Signal flow graph etc.
3	To introduce fundamentals of time and frequency domain analysis.
4	To develop concept of stability in time and frequency domain.

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Construct the transfer function of a given physical system from its differential equation, block diagram, or signal flow graph representation.	Apply
CO2	Examine time response analysis, stability using Routh-Hurwitz criteria, Root Locus Technique.	Analyze
CO3	Inspect the system's behavior in time-domain and frequency-domain of the model using Bode Plot, Polar Plot, Nyquist criteria. Etc.	Analyze
CO4	Determine the system response using state Space modelling	Evaluate

Module	**Module Contents**	**Hours**
I	**Time response Analysis** Standard test signals, time response of second order system, steady state errors and error constants, design specifications of second order system. Preliminary design considerations of Compensators need of compensation, lead compensations, lag compensation, lag-lead compensation.	8
II	**Stability Analysis in Time Domain** Concept of stability, condition of stability, characteristic equation, relative stability, Routh-Hurwitz criterion, special cases for determining relative stability.	7
III	**Root locus techniques** Basic concept, rules of root locus, application of root locus technique for control systems.	6
IV	**Frequency Response Analysis** Polar-plots, Bode-plots, Nyquist stability criterion, gain margin, phase margin, effect of addition of poles and zeros on bode plots.	6

V	**Analysis of Feedback** Basic idea of feedback control systems. Error analysis. P, PI, PD, PID controllers, Introduction to Digital Control	7
VI	**Analysis of Control Systems in State – Space** Basic concepts of state, state variable and state models, transfer matrix, Controllability, observability, obtaining state space equations in canonical form	7

Textbooks	
1	Control System Engineering", I.J. Nagrath, M. Gopal, 5th Edition, New Age International Publications, 2008
2	Ogata K., Modern Control Engineering, Prentice-Hall of India Pvt Ltd., New Delhi, 3rd edition, 2000.
3	Franklin G.F., Powell J.D., Emami-Naeini A., Feedback Control of Dynamic Systems, Pearson, Upper Saddle River, New Jersey, 5th edition, 2006.

References	
1	Modern Control System", Dorf, Bishop, 12th Edition, Prentice Hall, 2013
2	"Feedback and Control Systems", Schaum's Outlines Series book, 2nd Edition, McGraw Hill Education, 2012.

Useful Links	
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CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3	2	1	1										
CO2	3		1	1										
CO3			1	1										
CO4		2	1	1										

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

TY Electronics
Semester VI

Walchand College of Engineering, Sangli

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AY 2025-26

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem VI
Course Code	7EN321
Course Name	Electromagnetic Engineering
Desired Requisites:	

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	# Hrs/week	30	20	50	100
		Credits: #			

Course Objectives	
1	To **understand** the electric fields, electric energy and potential.
2	To **understand** the magnetic flux and forces, energy stored in magnetic field.
3	To **develop** in-depth understanding of time-varying fields and electromagnetic waves.
4	To **study** the electromagnetic wave transmission methods like transmission lines, antennas and waveguides.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Explain** the principles of static and time-varying electric and magnetic fields.	Understand
CO2	**Compare** the behaviour of electromagnetic waves in free space and guided medium like two-wire transmission line.	Understand
CO3	**Solve** the problems on static and time-varying electromagnetic fields.	Apply
CO4	**Analyze** the effects of electromagnetic radiation and electromagnetic interference.	Analyze

Module	**Module Contents**	**Hours**
I	**Electrostatics** Review of vector analysis and coordinate systems. Coulomb's Law, electric fieldintensity, field due to line charge, sheet charge; electric flux density, Gauss's Law and it's applications, divergence theorem; energy and potential, potentialgradient, electric dipole; energy density in electrostatic field	4
II	**Conductors, Dielectrics and Capacitance** Current and current density, continuity of current, conductor properties and boundary conditions; boundary conditions for perfect dielectric materials, Poisson's and Laplace's equations; Capacitance.	8
III	**Steady Magnetic Field** Magnetic field intensity, Biot-Savart Law, Ampere's circuital Law, Stokes' theorem, magnetic flux and magnetic flux density; scalar and vector magnetic potential; Force on a moving charge, force between differential current elements, properties of magnetic materials, energy stored in magnetic field, forces on magnetic materials, inductance, magnetic boundary conditions.	8
IV	**Time Varying Fields and Maxwell's Equations** Faraday's Law, displacement current, Maxwell's equations in point (differential) form and integral form, time varying potentials, time-harmonic fields	8

V	**Uniform Plane Electromagnetic Waves** Wave propagation in free space and dielectrics, Power flow in uniform plane wave, Poynting's theorem, wave propagation in conductors: skin depth, reflection of plane waves, standing wave ratio, polarization of uniform plane waves.	7
VI	**Transmission Lines** Types of two-conductor transmission lines, equivalent circuit, transmission line parameters, transmission line equations, lossless propagation, wave reflection, standing waves and voltage standing wave ratio, reflection coefficient, Smith Chart.	4

Textbooks	
1	William H. Hayt and John A. Buck, "Engineering Electromagnetics", 7th Edition, Tata McGraw- Hill, 2007.
2	Matthew N. O. Sadiku, "Elements of Electromagnetics", 3rd Edition, Oxford University Press, 2007.
3	S. C. Mahapatra and Sudipta Mahapatra, "Principles of Electromagnetics", Tata McGraw-Hill, 2011.
4	
References	
1	E. C. Jordan & K. Balman, "Electromagnetic Waves and Radiating Systems", 2nd Edition, PHI, 2007.
2	David K. Cheng, "Field and Wave Electromagnetics", Pearson Education, 2015.
Useful Links	
1	https://nptel.ac.in/courses/108/106/108106073/
2	https://nptel.ac.in/courses/108/104/108104087/

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1		2											2	
CO2		2		1									2	
CO3	3												2	
CO4	3			2									2	

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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Course Information	
Programme	B. Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem - VI
Course Code	7EN322
Course Name	Digital Communication
Desired Requisites:	Communication Engineering

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
		Credits: #			

Course Objectives	
1	To discuss in detail about information theory which allows us to analyze and characterize the fundamental limits on communication systems.
2	To explain various approaches of error control coding techniques
3	
4	

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Analyse performance of channel using information theory.	Analyzing
CO2	Illustrate various source coding technique.	Applying
CO3	Discuss error control coding techniques to improve	Evaluating
CO4	Analyze performance of spread spectrum communication system	Analyzing

Module	**Module Contents**	**Hours**
I	**Review of Probability Theory** Random Variable, cumulative distribution function, probability density function, random variable, Bivariate random variable, joint and conditional probabilities.	6
II	**Entropy, Relative Entropy, and Mutual Information** Entropy, Joint Entropy and Conditional Entropy, Relative Entropy and Mutual Information, Measure of Information. Avg. and Mutual Information. Joint and conditional entropy, Rate of Information	6
III	**Channel Capacity and Source Coding** Need, Source coding theorem, fixed length coding, variable length coding, kraft Inequality, Huffman Codes, Optimality of Huffman Codes, Shannon- Fanno coding technique, comparative study of source coding technique, AWGN channel capacity, resources of AWGN channel, Linear time invariant Gaussian channels, capacity of fading channels.	6

IV	**Linear Binary Block Codes** Introduction, Generator and Parity-Check Matrices, Repetition and Single-Parity-Check Codes, Binary Hamming Codes, Error Detection with Linear Block Codes, Weight Distribution and Minimum Hamming Distance of a Linear Block Code, Hard-decision and Soft-decision Decoding of Linear Block Codes, Cyclic Codes, Parameters of BCH and RS Codes, Interleaved and Concatenated Code	7
V	**Convolutional Codes** Convolutional codes – code tree, trellis, state diagram - Encoding – Decoding: Sequential search and Viterbi algorithm – Principle of Turbo coding	7
VI	**Spread Spectrum Technology** Introduction to spread spectrum, spread spectrum techniques, Direct sequence system, frequency hopping system, pulse FM (chirp) system, hybrid systems, Coding for communication and ranging- Property of codes for spread spectrum, Autocorrelation and cross correlation of codes, composites codes, code selection and signal spectra, error detection and correlation codes.	7

Textbooks	
1	K. Sam Shanmugam, “Digital and Analog Communication Systems” Willey India Pvt Ltd, 1996.
2	Simon Haykin, “Digital Communication”, Willey India Pvt Ltd, 2008.
3	
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References	
1	Bernard Sklar, “Digital Communications- Fundamentals and Applications”,SecondEdition, Pearson Education, 2016, ISBN: 9780134724058.
2	Error Correction Coding, Todd K Moon,Wiley Std. Edition, 2006
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Useful Links	
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CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3												3	
CO2		3												
CO3	3		3											3
CO4				3										3

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2025-26

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem VI
Course Code	7EN323
Course Name	Digital System Architecture
Desired Requisites:	Digital Electronics

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
		Credits: 3			

Course Objectives	
1	To explain the designs of building blocks of digital system viz. data path design, control unit design, memory units to finally design the microprocessor 2. 3. 4. 5.
2	To illustrate the concepts behind designing the robust digital systems.
3	To unfold the architectures of DACs and ADCs using various approaches motivating students to compare their performance.
4	To assign medium complexity digital system design related problems in batches as a self study exercise.
	To illustrate HDL implementation of digital designs in FPGA

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Explain the architectures of FPGAs and the concept behind programmable devices	Understand
CO2	Apply FSM approach to develop sequential digital circuits, and floating point and fixed point arithmetic to develop architectures of floating/fixed pointdata-path blocks.	Apply
CO3	Analyze digital circuits and their architectures for functionality, and memory units for timing performance using timing diagrams.	Analyze
CO4	Compare various approaches of designing memory blocks, DACs and ADCs with references to their merits and demerits and performance parameters respectively	Evaluate
CO5	Develop architectures of digital blocks (Data-path, Control units) with knowledge of functionality extending further to 4-bit/8-bit microprocessor with defined set of instructions.	Create

Module	**Module Contents**	**Hours**
I	**Designing Datapath Blocks** Number representation (fixed point and floating point), Fixed Pont arithmetic, floating point arithmetic, High speed adders/ Multipliers (Robertson's algorithm and Booth's algorithm), pipeline processing.	8

II	**Designing Control units** Concepts, Hardwired Control, Examples on hardwired control (Multiplier control unit), CPU control unit, Microprogrammed Control Unit, Example based on micro-programmed control unit, Concepts in Pipeline control	6
III	**Designing Memory Blocks** ROM, Internal Structure, Rom control inputs and timing, Static RAM, Internal Structure, Timing, Dynamic RAM, Timing, Memory Systems (Multilevel memories, Address translation, replacement policies), Caches (Address mapping, Associative, Direct and set-associative mapping), Cache performance	7
IV	**Processor Design** Introduction, Microcomputer Organization, Microprocessor Organization, Set of Instructions, Addressing Modes, Designing instruction, stack, subroutines and interrupt, Input-Output interface, Serial and parallel communication with processor, Direct Memory Access	6
V	**PLDs and Their Architectures** Introduction to Programmable Logic Devices, Field Programmable Gate Arrays, FPGA Architectures (Xilinx Spartan Series, Altera Stratix Series) involving Configurable Logic Blocks, I/O blocks, Programmable interconnects.	4
VI	**Data Converters**: **DAC** Binary weighted Resistor, R/2R ladder, Performance metrics of DAC (Resolution, settling time, linearity, speed, and Errors) **ADC** – Flash ADC, Successive Approximation ADC, Single slope ADC, Dual Slop ADC, ADC specifications (Quantization error, Intergral non-linearity error, Gain and Offset Error, Signal to Noise Ratio, Dynamic Range, Effective number of bits, Bit Error Rate, Figure of Merit)	9

Textbooks	
1	*Morris Mano, "Digital Logic and Microprocessoor Design", PHI, 2001*
2	John Wakerley, "Digital Design , Principles and Practices", PHI, 2005 3.
3	Hayes, "Computer Architecture and Organization", McGraw Hill, 3rd Edition, 2012
References	
1	Frank Vahid "Digital Electronics" Wiley Publication. 2012
2	Enoch O. Hwang, "Digital Logic and Microprocessoor Design with VHDL", Thomson Publication, 2007 Reprint
Useful Links	
1	www.xilinx.com
2	www.altera.com

CO-PO Mapping														
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1		2												
CO2	3													

CO3		3												
CO4		3												
CO5			3			1	1							3
The strength of mapping is to be written as 1: Low, 2: Medium, 3: High Each CO of the course must map to at least one PO.														

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli

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AY 2025-26

Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem VI
Course Code	7EN371
Course Name	Digital Communication Lab
Desired Requisites:	Digital Communication, Probability and Statistics

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**ESE**	**Total**
Tutorial	-	30	30	40	**100**
Practical	2 Hrs/Week				
Interaction	-	**Credits: 1**			

Course Objectives

1	To learn the principles and applications of information theory in communication systems
2	To Understand the current state of the art for both data compression and channel coding

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Apply different source coding techniques	Apply
CO2	Design various coding schemes for text, speech and audio.	Create
CO3	Design error control coding techniques	Apply
CO4	Apply methods to improve performance of digital communication system in presence of noise.	Apply

List of Experiments / Lab Activities

List of Experiments:

1. To find information and entropy of a given source.
2. Determination of various entropies and mutual information of the Binary Symmetric Channel.
3. Implementation of Shannon fanno source coding algorithm
4. Implementation of Huffmann source coding algorithm
5. Coding and decoding of Linear block codes
6. Coding and decoding of Hamming codes
7. Coding and decoding Convolutional codes
8. Case study example : Application of algorithm on text, speech and audio

Text Books

1	R. J. McEliece, "The Theory of Information and Coding", Cambridge Uinversity Press
2	Todd k Moon, "Error Correction Coding: Mathematical Methods and Algorithms",Wiley,2005
3	
4	

References

1	Bose, "Information Theory, Coding and Cryptography", Mcgrawhill Education

2	Joy A. Thomas, Thomas M. Cover, “Elements of information theory”, Wiley-Interscience; 2edition 2006.
3	
4	
Useful Links	
1	
2	
3	
4	

CO-PO Mapping															
	Programme Outcomes (PO)												**PSO**		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	1				3								1		
CO2	1				2									2	
CO3					3										
CO4					3										
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.															

Assessment				
There are four components of lab assessment, LA1, LA2, LA3 and LA4 IMP: LA4 is a separate head of passing. LA4 is treated as End Semester Exam and is based on all experiments/lab activities.				
Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40
Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.				

Walchand College of Engineering, Sangli

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Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem -VI
Course Code	7EN372
Course Name	Digital System Architecture Lab
Desired Requisites:	Digital Electronics Lab

Teaching Scheme		**Examination Scheme (Marks)**			
Practical	2 Hrs/ Week	**LA1**	**LA2**	**Lab ESE**	**Total**
Interaction		30	30	40	100
		Credits: 2			

Course Objectives	
1	To know the HDL language for Digital Design
2	To understand the difference in HDL and other high level programming language
3	To understand the concept in simulation and synthesis

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	The students will be able to design the basic digital circuits and test them.	Understand
CO2	Able to develop designed circuit using VHDL	Apply
CO3	Able to implement the control unit using VHDL	Analyse

List of Experiments / Lab Activities/Topics

VERILOG: Introduction to VERILOG, Program structure, Attributes, Functions and Procedures, Types of VERILOG architectures(Structural, Data flow, Behavioral), VERILOG concurrent and sequential constructs, Combinational and Sequential logic design using Verilog

List of Lab Activities:

1 Introduction to Xilinx with sample experiment in Verilog
2 1 bit full adder using 1 bit half adder as a component
3 4 bit full adder using 1 bit full adder as a component.
4 1 bit full adder using 8:1 multiplexer as component
5 1 bit full adder using 1:8 demux as component
6 Implementation of 4:1 mux using 2:1 mux as a component
7 Implementation of demultiplexer IC 74138
8 4 bit comparator
9 Implementation of flip flops
10 4-bit Counter using D-f/f
11 Counter using operators
12 UP counter and DOWN counter
13 Shift registers
14 Universal Shift register

Textbooks	
1	Douglas Perry , "VERILOG", , Tata McGraw-Hill,
2	Charles H Roth, "Digital System Design Using VHDL", Cengage Learning India
References	
1	Steafan,"Fundamentals of Digital Logic Using VERILOG ", McGraw Hill
2	Manjita Srivastava ,"Digital Design: HDL-Based Approach",,Cengage Learning India
Useful Links	
1	www.xilinx.com
2	www.altra.com

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2		3												
CO3						1	1							2

The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO, and preferably to only one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%

Assessment	Based on	Conducted by	Typical Schedule	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40

Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.

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AY 2025-26

Course Information	
Programme	B. Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem VII
Course Code	7EN332
Course Name	Professional Elective 2 -Real Time Operating System
Desired Requisites:	C programming, Embedded System Design

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial		30	20	50	100
		Credits: 3			

Course Objectives	
1	To make students familiar with installation and use of the Linux/ Embedded Linux operating system.
2	To give exposure for Embedded Linux boards as per the industry trends
3	To explain /demonstrate services provided by RTOS and their usage
4	To illustrate/demonstrate how to design of applications using RTOS. (uCOS-II)

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Illustrate various OS, Linux commands, Embedded Linux Board and concepts of RTOS	Understand
CO2	Develop programs by applying the knowledge acquired in Linux/ RTOS	Apply
CO3	Design the tasks and their interactions by using appropriate RTOS services for multitasking based (RTOS based) embedded system	Create
CO4	Implement Inter task communication using mailbox, semaphore, and Queue in RTOS	Apply

Module	**Module Contents**	**Hours**
I	Introduction to Operating System: Introduction to OS, Types of OS, Comparison of different OS, Linux Distributions, Linux architecture, Linux Kernel, File Systems, Shell utility, Installation and Configuration of Linux, Basic commands of Linux, Application programming in Linux, multifile programming	6
II	Introduction to Embedded Linux: Embedded Linux introduction, Why Embedded Linux? Linux vs. Embedded Linux, Components of Embedded Linux Systems, Embedded Linux Boot Flow Process, Embedded Linux Boards- Raspberry Pi /Beagle Bone, Raspberry Pi / Beagle Bone - OS installation and configuration, Facilities in Embedded Linux Boards used in Industry/Market	7
III	Introduction to Real-time OS and Real Time system contents RTOS Introduction, Foreground/Background Systems, Pre-emptive and Non-Pre-emptive Kernels, Priority inversion, Deadlock	7
IV	Task Management in RTOS: Task structure, RTOS initialization, Task stack, Task states and task state transitions. Creating and deleting a task, Task priority, Case studies of task-based applications.	7

V	Time and Event management in RTOS Clock tick, delaying a task, resuming the delayed task, getting system time, case study of application based on time management	7
VI	Intertask Communication in RTOS Need of Intertask communication, Semaphore, Mailbox, Queues in RTOS. Internals of RTOS for managing tasks and Intertask communication, Case study of RTOS applications.	6

Textbooks	
1	"MicroC OS II: The Real Time Kernel" Jean J. Labrosse, CMP books publication ISBN: 978-1578201037
2	"Mastering Embedded Linux Programming", Second Edition, Chris Simmonds.
3	"Simple Real-time Operating System: A Kernel," Chowdary Venkateswara Amazon, ISBN: 978-1425117825
4	"Real-Time Concepts for Embedded Systems," Qing Li, Caroline Yao Elsevier ISBN: 978-1578201240032
References	
1	https://www.engineersgarage.com/embedded-linux-tutorial-basics/
2	Exploring Raspberry Pi: Interfacing to the Real World with Embedded Linux" first Edition, Derek Molloy
3	https://freertos.org/Documentation/161204_Mastering_the_FreeRTOS_Real_Time_Kernel, A_Hands-On_Tutorial_Guide.pdf
4	www.micrium.com for uCOS-II related documents, tutorials, downloads.
Useful Links	
1	https://www.linux.org/.
2	www.nxp.com for processor specific documents
3	www.NPTEL.org for OS and RTOS related video courses
4	

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2		3												2
CO3			2											2
CO4			2										2	

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High

Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.

MSE shall be typically on modules 1 to 3.

ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.

ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.

For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

AY 2025-26

Course Information	
Programme	B. Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem,-VI
Course Code	7EN331
Course Name	Professional Elective-2: Digital Image Processing
Desired Requisites:	Digital Signal Processing

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	2 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
		30	20	50	100
		Credits: 3			

Course Objectives	
1	To develop an overview of the field of Image processing
2	To illustrate the fundamental algorithms and their implementation
3	To apply image processing algorithms for real problems

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Apply Digital Image Processing Techniques for gray scale images and colour images	Apply
CO2	Analyze various image segmentation techniques	Analyze
CO3	Explain image restoration, de noising and image compression techniques	Evaluate
CO4	Identify image representation and description techniques	Understand

Module	**Module Contents**	**Hours**
I	**Introduction to Digital Image Processing** Fundamental steps in digital image processing- Components of Image processing system Image sensing and acquisition - Image sampling and Quantization - relationship between pixels. Image file formats	**3**
II	**Image enhancement Techniques** Spatial Domain: Gray level transformation - Histogram processing, Spatial filtering - smoothing filters, sharpening filters; Frequency Domain: Fourier transform – smoothing frequency domain filters, sharpening filters, Homographic filtering	**5**
III	**Image Restoration, Denoising and Image Compression Techniques** Model of Image degradation/ restoration process Types of image blur- Noise models, Classification of Image restoration techniques, Blind de convolution, Image de noising, Median filtering, Inverse filtering, Weiner, least square, Geometric mean filters; Classification of compression techniques, Fundamentals of Information Theory, Shannon Fano coding, Huffman coding, Transform based compression	**5**
IV	**Color Image Processing** Color fundamentals, color models, pseudo color image processing, basics of full–color image processing, color transforms, smoothing and sharpening, color segmentation	**5**

V	**Image Segmentation** Classification of Image segmentation Techniques, Region approach to Image segmentation, Edge based segmentation, Classification of edges, edge detection, edge linking, Hough Transform, Clustering Techniques, Watershed Transformation.	**5**
VI	**Representation & Description** Chain codes - Polygonal Approximations – signatures - Boundary segments - Skeletons; Boundary Descriptors - Regional descriptors	**4**
Textbooks		
1	Digital Image Processing", R.C. Gonzalez and R.E. Woods, 3rd Edition, Prentice-Hall	
References		
1	Fundamentals of Digital Image Processing - A.K. Jain	
Useful Links		
1	NPTEL	

	CO-PO Mapping													
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													2
CO2		3												2
CO3				2										2
CO4	2													2

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech. Sem. VI
Course Code	7EN333
Course Name	Professional Elective 2- Internet of Things
Desired Requisites:	Electronics Instrumentation, Embedded System

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	2 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives

1	To introduce the fundamentals, challenges, and enabling technologies of the Internet of Things (IoT)
2	To familiarize students with IoT networking protocols, M2M communication, and system architectures.
3	To provide understanding of security aspects, cloud integration, and data analytics in IoT.
4	To explore real-world applications of IoT through case studies in smart environments.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Describe** the fundamental concepts, challenges, and enabling technologies of IoT.	Understand
CO2	**Compare** and **analyze** various IoT protocols and M2M communication architectures.	Analyze
CO3	**Explain** IoT security threats and **suggest** appropriate mitigation techniques.	Analyze
CO4	**Interpret** cloud-based IoT architectures and evaluate real-world applications using case studies.	Evaluate

Module	**Module Contents**	**Hours**
I	**IoT Fundamentals and Challenges:** Definition and Characteristics of IoT, Design considerations of IoT, IoT enabled Technologies, Applications of IoT	3
II	**Networking Fundamentals and protocols**: TCP/IP Fundamentals, Connectivity and communication technologies for IoT: IEEE 802.15.4, 6LowPAN, RFID, Wireless HART, MQTT, CoAP, XMPP, AMQP, LORA, Role of Gateways and Middleware in IoT,	4
III	**Machine to Machine communication**: M2M features, Hardware and software architecture of sensor node, Node types, Ecosystem, various M2M platforms, Power Optimization and harvesting	4
IV	**IoT Security**: IoT Vulnerabilities, Threats and risk, Firewalls data security, Common attacks. Risk Assessment and Mitigation Strategies, Encryption, Authentication, and Blockchain in IoT	3

V	**Sensor Cloud and Data Analytics Fundamentals**: cloud computing and virtualization concepts, Cloud Architecture, Cloud computing, benefits , challenges, risks Cloud services , introduction to software defined network, Role of Data Analytics in IoT.	3
VI	**IoT Applications :** IoT Case Studies with Cloud: Smart cities, Smart Homes, Smart Agriculture, Smart Energy, Smart vehicles	3

Text Books	
1	Sudip Misra, Chandana Roy, Anandarup Mukherjee, "Introduction to Industrial Internet of Things and Industry 4.0" 2021

References	
1	D.E. Comer "Internetworking with TCP/IP", Vol. I (4th Edition), II, III (PHI)
2	Olivier Hersent, David Boswarthick "Internet of Things Applications and Protocols ", Wiely publication 2nd Ed.
3	William Stallings "Foundations of Modern Networking : SDN, NFV, QoE, IoT and Cloud" Pearson Education

Useful Links	
1	https://onlinecourses.nptel.ac.in/noc21_cs17/preview

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3	1	1										3	
CO2		3		3	2									2
CO3		3		3	3								1	3
CO4			2	2	3								1	

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3.

ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.

ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.

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Course Information	
Programme	B. Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem VI
Course Code	7EN373
Course Name	Digital Image Processing Lab
Desired Requisites:	Digital Signal Processing

Teaching Scheme		**Examination Scheme (Marks)**			
Practical	2 Hrs/ Week	**LA1**	**LA2**	**Lab ESE**	**Total**
		30	30	40	100
		Credits: 1			

Course Objectives

1	To learn digital image processing techniques and apply in practical problems using MATLAB

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Demonstrate basic operations of Digital Image Processing in spatial domain	Explain
CO2	Model frequency domain analysis of digital images	Apply
CO3	Apply image restoration and de noising techniques to image	Utilize
CO4	Perform color image processing	Demonstrate

List of Experiments / Lab Activities/Topics

List of Lab Activities:

1. **Image Operations in spatial domain**
   - Brightness Enhancement
   - Brightness Suppression
   - Contrast Manipulation
   - Histogram Equalization
   - Determination of Image Negative
   - Threshold Operation
   - Gray level slicing without preserving background
   - Gray level slicing with background
   - Logarithmic Transformation
   - Power Law Transformation
   - Spatial domain Filtering
   - Noise minimization using averaging filter
   - Noise minimization using median Filter
   - Un-sharp masking
   - Bit-plane slicing
2. **Image Operations in Frequency domain**
   - Low pass filter
   - High pass filtering
   - Band pass filter
3. **Image Arithmetic**
   - Addition
   - Subtraction
   - Multiplication
   - Division
   - Blending
   - Histogram Equalization
   - Histogram Specification
4. **Image Restoration and denoising**
   - Create motion blur
   - Inverse filtering
   - Psudo inverse filter
   - Wiener filter
5. **Colour Image Processing**
   - Extraction of Red Green and Blue Components of colour image
   - Removal of RGB Plane
   - Histogram of a colour image
   - Histogram equalization of a colour image
   - Various types of filtering of a colour image
   - Pseudo-colouring Operation

Textbooks	
1	"Digital Image Processing Using MATLAB ", R.C. Gonzalez and R.E. Woods, 3rd Edition, Prentice-Hall
References	
1	Fundamentals of Digital Image Processing - A.K. Jain
Useful Links	
1	NPTEL

CO-PO Mapping														
	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													2
CO2		3												2
CO3				2										2
CO4	2													2
The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High Each CO of the course must map to at least one PO, and preferably to only one PO.														

Assessment				
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%				
Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40
Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.				

Walchand College of Engineering, Sangli

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Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem VI
Course Code	7EN374
Course Name	Real Time Operating System Lab
Desired Requisites:	Theory/Lab Courses with C programming, Microcontroller Peripherals and Interfacing, Embedded System Design.

Teaching Scheme		**Examination Scheme (Marks)**			
Practical	2 Hrs/ Week	**LA1**	**LA2**	**Lab ESE**	**Total**
Interaction	-	30	30	40	100
		Credits: 1			

Course Objectives

1	To learn system Architecture, configuration, and Programming for Embedded Linux Based System.
2	To facilitate students to gain practical experience of RTOS and services provided by it.
3	To help students to co-relate the RTOS theory with the RTOS implementation.
4	To provide exposure to industry applications and facilitate for writing applications using Linux and RTOS.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Installation of OS Process and write programs / scripts for Embedded Linux Board.	Apply
CO2	Verify the RTOS fundamentals, through illustrative programs and demonstrate usage of task, time, and event management, using a simulator. (Programming skill, Modern Tools)	Analyze
CO3	Design and implement RTOS-based applications utilizing semaphores, mailboxes, and queues for task synchronization and shared resource management using simulator.	Evaluate
CO4	Implement a given logic as an RTOS based application. Create document of the same and demonstrate using simulation tools. (Programming skill, Independent and teamwork, Modern Tools)	Create

List of Experiments / Lab Activities/Topics

List of Lab Activities:

1. Experiments to revise an Embedded System Design
2. Experiment to study Linux distribution installation, configuration and basic commands of it.
3. Experiment to study configuration for an Embedded Linux Board.
4. Experiment to access GPIO of an Embedded Linux Board to control components / devices interfaced to it.
5. Demonstration of RTOS based application in keil micro vision
6. Writing of RTOS based application.
7. Finding the type of kernel for a given RTOS (Pre-emptive or Non-pre-emptive)
8. Semaphore for managing shared resource and task synchronization
9. Demonstration of Clock tick and its effect of event timing in RTOS based systems.
10. Semaphore for event synchronization
11. Using mailbox facility in RTOS
12. Using queue facility in RTOS
13. Avoiding deadlock in RTOS

Textbooks	
1	Chris Simmonds , “Mastering Embedded Linux Programming”, Second Edition.
2	Derek Molloy ,“Exploring Raspberry Pi: Interfacing to the Real World with Embedded Linux” first Edition,
3	Jean J. Labrosse, “MicroC OS II: The Real Time Kernel” CMP books publication ISBN: 978-1578201037

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Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem. VI
Course Code	7EN375
Course Name	Professional Elective II -Internet of Things Lab
Desired Requisites:	Sensors and Instrumentation, Embedded System

Teaching Scheme		**Examination Scheme (Marks)**			
Practical	2 Hrs/ Week	**LA1**	**LA2**	**Lab ESE**	**Total**
Interaction	- Hrs/ Week	30	30	40	100
		Credits: 1			

Course Objectives

1	To provide understanding of the Internet of Things concepts.
2	To demonstrate sensor node architecture and communication.
3	To understand applications of Internet of Things and its usefulness for society.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Design sensor node	Apply
CO2	Compare various connectivity and communication technologies	Analyze
CO3	Simulate/Design applications for solution building in IoT domain	Create

List of Experiments / Lab Activities/Topics

List of Lab Activities:

1. Introduction to IoT Devices: Arduino, Raspberry Pi, Node-MCU, etc.
2. Sensor Interfacing:
   Different sensors with IoT devices.
   Collecting sensor data and displaying it on the device
3. Actuator Control:
   Controlling actuators using IoT devices.
4. Data Logging and Visualization:
   Logging sensor data on IoT devices or cloud platforms. sensor data using graphs or web interfaces
5. Handling Cloud Database
6. IoT Energy Management: Optimizing power consumption through sleep modes, duty cycling, and low-power components, Implementing basic security measures for IoT devices
7. Use of IoT public cloud for data storage and processing
8. Mini Project based on All labs.

Textbooks

1	"Introduction to Industrial Internet of Things and Industry 4.0" Sudip Misra, Chandana Roy, Anandarup Mukherjee 2021

References

1	"Internet of Things Applications and Protocols ", Wiely publication 2nd Ed.
2	William Stallings "Foundations of Modern Networking: SDN, NFV, QoE, IoT and Cloud" Pearson Education

Useful Links	
	-

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1			3											2
CO2				3										
CO3					3				3				2	

The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO, and preferably to only one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing (min 40 %), LA1+LA2 should be min 40%

Assessment	Based on	Conducted by	Typical Schedule	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40

Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.

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Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Third Year B. Tech., Sem-VI
Course Code	7CEEN345
Course Name	Mini Project (Field Project)
Desired Requisites:	ECAD, ICA, Digital Signal Processing, Embedded System Design, Digital Signal Processing

Teaching Scheme		**Examination Scheme (Marks)**			
Practical	2 Hrs/ Week	**LA1**	**LA2**	**Lab ESE**	**Total**
Interaction	-	30	30	40	100
		Credits: 1			

Course Objectives

1	To provide students hands on experience on, troubleshooting, maintenance, fabrication, innovation, record keeping, documentation etc. thereby enhancing the skill and competency part of technical education.
2	To create an Industrial environment and culture within the institution.
3	To inculcate innovative thinking and practice based learning and thereby preparing students for their final year project.
4	To set up self-maintenance cell within departments to ensure optimal usage of infrastructure Facilities.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Choose, Initiate, and manage a minor project.	Understand
CO2	Propose research problem and present it in a clear and distinct manner through different oral, written and design techniques.	Apply
CO3	Construct the circuit using hardware and/or software.	Create
CO4	Execute the project and comment upon the results of it.	Analyze

List of Experiments / Lab Activities/ Topics

Mini Project Description:

A project group shall consist of normally 3 students per group. The mini project will involve the design, construction, and debugging of an electronic system approved by the department. Each student should conceive, design and develop the idea leading to a project/product. **The theme of the project should be related to electronics engineering discipline to be decided by the students based on the societal needs after an exhaustive survey.**

Each student must keep a project notebook/logbook. The project notebooks will be checked periodically throughout the semester, as part of in-semester-evaluation. The student should submit a soft bound report at the end of the semester. The final product as a result of mini project should be demonstrated at the time of examination.

Textbooks

1	Electronics Projects For Dummies, by by Earl Boysen and Nancy Muir, Published by Wiley Publishing, Inc., 2006
2	Make: Electronics, by Charles Platt, Published by Maker Media, 2015

3	
4	
References	
1	A. E. Ward, J.A.S. Angus, “Electronic Product Design”, Stanley Thrones (Publishers) Limited, 1996.
2	Paul Horowitz, Winfield Hill, “The Art of Electronics”, Cambridge University Press, 1989
3	
4	
Useful Links	
1	
2	
3	
4	

CO-PO Mapping														
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3	3								2	2			2
CO2			3		2									
CO3			3		2						1		1	1
CO4		2							3	3				
The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High Each CO of the course must map to at least one PO, and preferably to only one PO.														

Assessment				
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Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40
Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.				